Monolithic Time-to-Digital Converter with 20ps resolution

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Abstract

We present a fully-integrated Time-to-Digital Converter, in a standard 0.8µm-CMOS technology, based on a cyclic pulse-shrinking design, that provides the lowest channel width of 20ps ever reported in literature for single-shot measurements performed by monolithic circuits, with differential linearity errors lower than 10ps (less than 0.5LSB), conversion time shorter than 20µs, and 18ns Full-Scale-Range.

1. Time-intervals measurements

Measurement and digitalization of time intervals with very high resolution and accuracy has great importance in applications such as Time-Correlated Single-Photon-Counting [1, 2], optical characterization of CMOS circuits [3] and laser-ranging [4]. In many applications, a Start trigger, usually synchronous with the excitation (e.g. by means of a laser pulse) of a target (e.g. a biological sample), is followed by a Stop pulse from a detector (e.g. a photodiode): the delay between the two must be accurately measured with picoseconds resolution. In other applications the time-delay to measure is the width of a pulse, from its rising to its falling-edge. In the following, Full-Scale-Range (FSR) means the maximum duration to be measured and channel-width is the minimum time difference that yields a digital output that differs of the Least-Significant Bit (LSB).

Traditionally, very short (nanosecond-scale or less) time-interval are measured by means of Time-to-Amplitude Converter (TAC) modules followed by Analog-to-Digital Converter (ADC) boards. The resulting equipment is usually bulky and very difficult to integrate, if very good performances are to be guaranteed. Time-to-Digital Converters (TDC) are alternative solutions that directly provide the output digital coding of the measurement, with no intermediate analog conversion [5]. TDCs are mainly based on delay lines, in which signals to be measured propagate [6]-[10], attain channel widths of hundreds of picoseconds and usually suffer from poor linearity, caused by mismatches among delay line stages.

Another approach for TDCs is the pulse-shrinking technique, where pulses to be measured are repeatedly shortened: the number of cycles needed to make the pulse "disappear" is the output coding. Linear pulse-shrinking TDCs [11] have been demonstrated, but suffer from limited accuracy due to mismatches.

In order to account for mismatches, a different cyclic structure was proposed [12, 13], able to reach 69ps-channel widths, by using only one stage for pulse shrinking, thus improving linearity.

In this paper we propose a fully-integrated TDC with channel widths down to few tens of picoseconds and with a linearity better than those previously reported, thanks to a fine tailoring of the design based on the analytical modelling of pulse shrinking herewith reported.

2. Pulse shrinking

The basic functional blocks of the cyclic pulse-shrinking TDC are depicted in Fig.1. The pulse to be measured is launched into a loop of inverters, through a Coupling input Stage. If all inverters were equal, the pulse will maintain its duration, regardless the number of loops made within the ring. Now, let’s suppose that one inverter differs from the others. As will be discussed in depth later, this will result in either a pulse shrinking or enlargement. In the former case, the pulse will reduce its duration at every cycle in the loop, until disappearing. By counting the number of iterations before the pulse vanishes, it is possible to determine its original length.

It should be noticed that, with such an approach, since only one element of the TDC is responsible for the pulse shrinking, a very good linearity is achievable, regardless of mismatches introduced by process tolerances. Instead, this is not true with the linear pulse shrinking approach, in which shrinking is provided by a set of different elements [11].

Pulse shrinking is achieved by way of one gate that differs from all the others (all identical), for instance in the rising or falling time (these two can not be equal), as shown in Fig. 2. Such difference can be obtained either by simply designing proper aspect ratio W/L for the MOS transistors, or by means of a third transistor put in series with the NMOS, the PMOS or both, acting as a...
Fig. 2 Effect of a different gate on the pulse width.

resistor [11],[12]: by varying its gate voltage, the amount of the shrinking can be tailored. Despite of the flexibility of such solution, the need of a very precise and stable external reference voltage introduces problems of linearity and jitter, making it necessary some sort of self-calibration.

Some simple mathematics can help in understanding the problem and for the correct design of the circuit. In Fig.2, where the different gate is only the second, let \( C_1 \), \( C_2 \) and \( C_3 \) be the input capacitances of the three inverters, \( k_{p1} \), \( k_{n1} \) the conductivity constants and the \( N \)-th transistor couple. If we suppose for simplicity that the input pulses at each inverter are ideally rectangular, the rising and falling times of the output of the first inverter are given by the following expression:

\[
\tau_{rl1} = \frac{2C_1V_{th}}{k_{n1}(V_{dd} - V_{th})} + \frac{C_1}{k_{n1}(V_{dd} - V_{th})} \ln \left( \frac{1.5V_{dd} - 2V_{th}}{0.5V_{dd}} \right)
\]

\[
\tau_{fl1} = \frac{-2C_1V_{th}}{k_{p1}(V_{dd} - V_{th})} + \frac{C_1}{k_{p1}(V_{dd} - V_{th})} \ln \left( \frac{1.5V_{dd} - 2V_{th}}{0.5V_{dd}} \right)
\]

Same expressions apply for the second inverter.

The amount of shrinking after the first, \( \Delta W_{1} = \tau_{fl1} - \tau_{rl1} \), and the second inverter \( \Delta W_{2} = \tau_{fl2} - \tau_{rl2} \), are given by:

\[
\Delta W_{1} = C_1 \left( \frac{1}{k_{p1}} - \frac{1}{k_{n1}} \right) \frac{2V_{th}}{(V_{dd} - V_{th})} + \frac{1}{(V_{dd} - V_{th})} \ln \left( \frac{1.5V_{dd} - 2V_{th}}{0.5V_{dd}} \right)
\]

\[
\Delta W_{2} = C_1 \left( \frac{1}{k_{p2}} - \frac{1}{k_{n2}} \right) \frac{2V_{th}}{(V_{dd} - V_{th})} + \frac{1}{(V_{dd} - V_{th})} \ln \left( \frac{1.5V_{dd} - 2V_{th}}{0.5V_{dd}} \right)
\]

Since \( C_1 = C_{rl} \), the total pulse shrinking, given by the sum \( \Delta W_{1} + \Delta W_{2} \), is [13]:

\[
\Delta W = \alpha \cdot \left[ C_1 \left( \frac{1}{k_{p1}} - \frac{1}{k_{n1}} \right) - C_1 \left( \frac{1}{k_{p2}} - \frac{1}{k_{n2}} \right) \right]
\]

where \( \alpha \) is a coefficient independent from the transistor dimensions (i.e. layout) equal to:

\[
\alpha = \frac{2V_{th}}{(V_{dd} - V_{th})} + \frac{1}{(V_{dd} - V_{th})} \ln \left( \frac{1.5V_{dd} - 2V_{th}}{0.5V_{dd}} \right)
\]

From Eq.(1) it is apparent that no pulse shrinking occurs if gates are all identical (i.e. \( C_1 = C_{rl}, k_{p1} = k_{n2} \) and \( k_{p2} = k_{n2} \)), or if the falling and rising times of the \( N \)-th gate are equal (\( k_{pN} = k_{nN} \)). Instead, the shrinking will take place every time the pulse passes through a different gate.

In the next Section we will show how the conditions highlighted in Eq.(3) affect the proper TDC design.

3. TDC Design

The cyclic pulse-shrinking TDC was fabricated in a standard double-metal double-poly 0.8μm-CMOS technology, with standard +5V supply. The typical rising and falling times of a symmetrical inverter with minimal dimensions are 300ps, with propagation delays of 200ps.

From Eq.(2), it is apparent that for the smallest channel width, it is necessary to minimize the variations in the different gates. On the other hand, process variability must be taken into account, therefore both conditions in Eq.(3) must be satisfied for the worst case, in order to have a reasonable assurance that pulses will not be enlarged rather than shrunk. For this reason careful simulations were made, often using corner analysis or Monte Carlo techniques. For instance Fig.4 shows the expected process-induced variations on the channel width in 200 samples of the proposed TDC.

We found that a reasonable choice is \( W/L_{p} = 1/0.8 \) and \( W/L_{n} = 4/0.8 \) for all the gates, apart from the two NORs with \( W/L_{p} = 1/1.08 \) and \( W/L_{n} = 10/0.8 \). The total number of inverters in the loop must be chosen in accordance to the required FSR. We decided to work with a FSR=18ns; since the propagation delay of each inverter is 200ps, 90 inverters are needed.
Fig. 4 Expected channel width distribution due to process-induced tolerances.

For counting the number of cycles necessary for the pulse to disappear, equal to its length divided by the channel width, we used a 16bit ripple counter, more than enough. According to simulations, it stands a working frequency of 60MHz, so it is perfectly able to follow the loop output pulses, every 90-200ps=18ns. Even if the counter will stop detecting pulses some cycles before they completely vanish, this effect will introduce a constant offset in the output coding, that is systematic and affects every measure in the same way. Therefore it can be compensated by a simple TDC calibration, that will also account for the anomalous shrinking that the loop introduces when the circulating pulse has a width comparable to its rising and falling times.

We added some additional circuitry to the TDC core. In particular, a simple input stage generates the pulse from the rising edges of two external signals, acting as the Start and Stop inputs of conventional TACs. In this way, the TDC can measure the time interval between the occurring of two independent signals, and not only the duration of a pulse.

The complete layout of the whole TDC is shown in Fig.5. The physical dimensions are 2mm x 1mm, mainly due to the area occupation of the counter’s pads. Indeed, the inverters loop has very tiny dimensions of 55μm x 450μm. A serial counter instead of the parallel one will reduce the chip area to less than a quarter.

As visible in Fig.5, the empty silicon estate can be used for other auxiliary electronics: the control logic for masking multiple Start or Stop pulses; the automatic reset after each conversion; the output flag at the end-of-conversion; and so on.

4. Experimental results

The TDC was tested using a simple testing board employing a microcontroller for the acquisition of the TDC’s output codes and the data downloading to a remote computer. Start-Stop time delay was generated by using a set of coaxial-cables to differently delay a triggering signal provided by the same microcontroller. In this way no jitter is introduced and repetitive measurements of the same time interval can be performed without affecting the overall accuracy. The linearity of the TDC was compared to that of a high linearity and low time jitter system composed by a TAC by Tennelec (mod.TC862), an ADC (mod.7423UHS) plus an MCA (Multi-Channel Analyzer, mod. Varro 8k) by Silena.

The measured TDC resolution, i.e., its channel width is 20ps; the FSR is 18ns and the maximum conversion time is 20μs, thus making possible a maximum counting rate up to 50kHz.

Figure 6 shows the measured distribution of the TDC output codes for repetitive measurements of the same time interval, that is a signature of the TDC precision.

Fig. 5 Layout of the developed TDC.

Fig. 6 Measured precision of the TDC at the middle of the FSR.

Fig. 7 Measured Differential-Non-Linearity.
The distribution has a root mean squared value of 3.8 LSB, corresponding to a Full-Width at Half Maximum of 8.5 channels.

Figure 7 shows how the Differential-Non-Linearity (DNL) is limited to below 0.5 LSB over the whole full-scale range.

5. Conclusions and perspectives

We realized a fully-integrated cyclic pulse-shrinking TDC with resolution down to 20ps, and differential-non-linearity errors below 10ps. Compared with other techniques reported in literature for integrated TDC, the proposed implementation results in low power consumption, simple design and no need for external adjustments (like Phase-Locked-Loop control of the loop round trip used in [7]-[10]).

By way of the reported analytical modelling of the pulse-shrinking effect (see. Eq.(3)), it is possible to tailor the TDC design on the technology worst cases parameters, in order to ensure the shortest channel width (highest TDC resolution) compatible to the fabrication process tolerances. Moreover, as shown in Eq.(2), we believe that channel widths shorter than the 20ps reported in our present TDC can be obtained by using a technology with minimum gate length shorter than 0.8μm.

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References